Bulletin I25172 rev. B 04/00

International
IOR Rectifier

ST303C..C SERIES

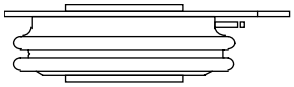
INVERTER GRADE THYRISTORS

Puk Version

620A

Features

- Metal case with ceramic insulator
- International standard case TO-200AB (E-PUK)
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- High surge current capability
- Low thermal impedance
- High speed performance



case style TO-200AB (E-PUK)

Typical Applications

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

Major Ratings and Characteristics

Parameters		ST303C..C	Units
$I_{T(AV)}$		620	A
	@ T_{hs}	55	°C
$I_{T(RMS)}$		1180	A
	@ T_{hs}	25	°C
I_{TSM}	@ 50Hz	7950	A
	@ 60Hz	8320	A
I^2t	@ 50Hz	316	KA^2s
	@ 60Hz	289	KA^2s
V_{DRM}/V_{RRM}		400 to 1200	V
t_q range (*)		10 to 30	µs
T_J		- 40 to 125	°C

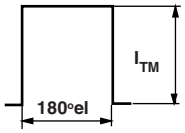
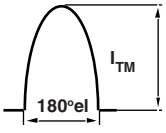
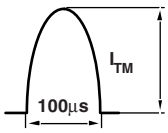
(*) t_q = 10 to 20µs for 400 to 800V devices
t_q = 15 to 30µs for 1000 to 1200V devices

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM}, maximum repetitive peak voltage V	V_{RSM}, maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J$ max. mA
ST303C..C	04	400	500	50
	08	800	900	
	10	1000	1100	
	12	1200	1300	

Current Carrying Capability

Frequency							Units
50Hz	1314	1130	2070	1940	6930	6270	A
400Hz	1260	1040	2190	1880	3440	2960	
1000Hz	900	700	1900	1590	1850	1540	
2500Hz	340	230	910	710	740	560	
Recovery voltage Vr	50	50	50	50	50	50	V
Voltage before turn-on Vd	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50	50	-	-	-	-	A/µs
Heatsink temperature	40	55	40	55	40	55	°C
Equivalent values for RC circuit	10Ω / 0.47µF		10Ω / 0.47µF		10Ω / 0.47µF		

On-state Conduction

	Parameter	ST303C..C	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current	620 (230)	A	180° conduction, half sine wave		
	@ Heatsink temperature	55 (85)	°C	double side (single side) cooled		
$I_{T(RMS)}$	Max. RMS on-state current	1180	A	DC @ 25°C heatsink temperature double side cooled		
I_{TSM}	Max. peak, one half cycle, non-repetitive surge current	7950	A	t = 10ms	No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max
		8320		t = 8.3ms		
		6690		t = 10ms	100% V_{RRM} reapplied	
		7000		t = 8.3ms		
I^2t	Maximum I^2t for fusing	316	KA^2s	t = 10ms	No voltage reapplied	
		289		t = 8.3ms		
		224		t = 10ms	100% V_{RRM} reapplied	
		204		t = 8.3ms		
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	3160	$KA^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied		

On-state Conduction

	Parameter	ST303C..C	Units	Conditions
V_{TM}	Max. peak on-state voltage	2.16	V	I_{TM}= 1255A, $T_J = T_J$ max, t_p = 10ms sine wave pulse
$V_{T(TO)1}$	Low level value of threshold voltage	1.44		(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.
$V_{T(TO)2}$	High level value of threshold voltage	1.48		(I > π x $I_{T(AV)}$), $T_J = T_J$ max.
r_{t1}	Low level value of forward slope resistance	0.57	mΩ	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.
r_{t2}	High level value of forward slope resistance	0.56		(I > π x $I_{T(AV)}$), $T_J = T_J$ max.
I_H	Maximum holding current	600	mA	T_J = 25°C, I_T > 30A
I_L	Typical latching current	1000		T_J = 25°C, V_A= 12V, Ra = 6Ω, I_G= 1A

Switching

	Parameter	ST303C..C		Units	Conditions
di/dt	Max. non-repetitive rate of rise of turned-on current	1000		A/µs	$T_J = T_J$ max, V_{DRM} = rated V_{DRM} I_{TM} = 2 x di/dt
t_d	Typical delay time	0.83		µs	T_J= 25°C, V_{DM} = rated V_{DRM}, I_{TM} = 50A DC, t_p= 1µs Resistive load, Gate pulse: 10V, 5Ω source
		Min	Max		
t_q	Max. turn-off time (*)	10	30		$T_J = T_J$ max, I_{TM} = 550A, commutating di/dt = 40A/µs V_R = 50V, t_p = 500µs, dv/dt: see table in device code

(*) t_q = 10 to 20µs for 400 to 800V devices; t_q = 15 to 30µs for 1000 to 1200V devices.

Blocking

	Parameter	ST303C..C	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	500	V/µs	$T_J = T_J$ max. linear to 80% V_{DRM}, higher value available on request
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current	50	mA	$T_J = T_J$ max, rated V_{DRM}/V_{RRM} applied

Triggering

	Parameter	ST303C..C	Units	Conditions
P_{GM}	Maximum peak gate power	60	W	$T_J = T_J$ max, f = 50Hz, d% = 50
$P_{G(AV)}$	Maximum average gate power	10		
I_{GM}	Max. peak positive gate current	10	A	$T_J = T_J$ max, $t_p \leq$ 5ms
$+V_{GM}$	Maximum peak positive gate voltage	20	V	$T_J = T_J$ max, $t_p \leq$ 5ms
$-V_{GM}$	Maximum peak negative gate voltage	5		
I_{GT}	Max. DC gate current required to trigger	200	mA	T_J = 25°C, V_A = 12V, Ra = 6Ω
V_{GT}	Max. DC gate voltage required to trigger	3	V	
I_{GD}	Max. DC gate current not to trigger	20	mA	$T_J = T_J$ max, rated V_{DRM} applied
V_{GD}	Max. DC gate voltage not to trigger	0.25	V	

Thermal and Mechanical Specification

	Parameter	ST303C..C	Units	Conditions
T_J	Max. operating temperature range	-40 to 125	°C	
T_{stg}	Max. storage temperature range	-40 to 150		
R_{thJ-hs}	Max. thermal resistance, junction to heatsink	0.09 0.04	K/W	DC operation single side cooled DC operation double side cooled
R_{thC-hs}	Max. thermal resistance, case to heatsink	0.020 0.010	K/W	DC operation single side cooled DC operation double side cooled
F	Mounting force, ± 10%	9800 (1000)	N (Kg)	
wt	Approximate weight	83	g	
	Case style	TO - 200AB (E-PUK)		See Outline Table

ΔR_{thJ-hs} Conduction

(The following table shows the increment of thermal resistence R_{thJ-hs} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction		Rectangular conduction		Units	Conditions
	Single Side	Double Side	Single Side	Double Side		
180°	0.010	0.010	0.007	0.007	K/W	$T_J = T_J$ max.
120°	0.012	0.012	0.012	0.013		
90°	0.015	0.015	0.016	0.017		
60°	0.022	0.022	0.023	0.023		
30°	0.036	0.036	0.036	0.037		

Ordering Information Table

Device Code

ST	30	3	C	12	C	H	K	1	
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩

1 - Thyristor

2 - Essential part number

3 - 3 = Fast turn off

4 - C = Ceramic Puk

5 - Voltage code: Code x 100 = V_{RRM} (See Voltage Rating Table)

6 - C = Puk Case TO-200AB (E-PUK)

7 - Reapplied dv/dt code (for t_q test condition)

8 - t_q code

9 - 0 = Eyelet term. (Gate and Aux. Cathode Unsoldered Leads)
1 = Fast-on term. (Gate and Aux. Cathode Unsoldered Leads)
2 = Eyelet term. (Gate and Aux. Cathode Soldered Leads)
3 = Fast-on term. (Gate and Aux. Cathode Soldered Leads)

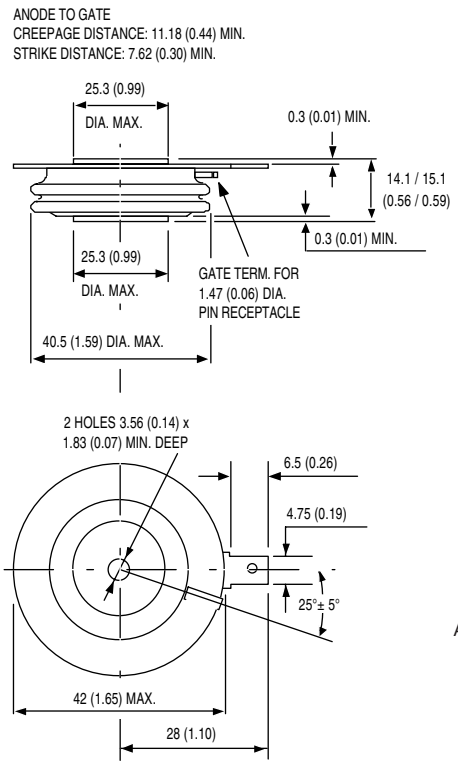
10 - Critical dv/dt:
None = 500V/µsec (Standard value)
L = 1000V/µsec (Special selection)

dv/dt - t_q combinations available

	dv/dt (V/µs)	20	50	100	**200**	400
t_q(µs) up to 800V	10	CN	DN	EN	**FN ***	HN
	12	CM	DM	EM	FM	HM
	15	CL	DL	EL	**FL ***	HL
	20	CK	DK	EK	**FK ***	HK
t_q(µs) only for 1000/1200V	15	CL	--	--	--	--
	18	CP	DP	--	**--**	--
	20	CK	DK	EK	**FK ***	HK
	25	CJ	DJ	EJ	**FJ ***	HJ
	30	--	DH	EH	FH	HH

*Standard part number.
All other types available only on request.

Outline Table



Case Style TO-200AB (E-PUK)

All dimensions in millimeters (inches)

Quote between upper and lower pole pieces has to be considered after application of Mounting Force (see Thermal and Mechanical Specification)

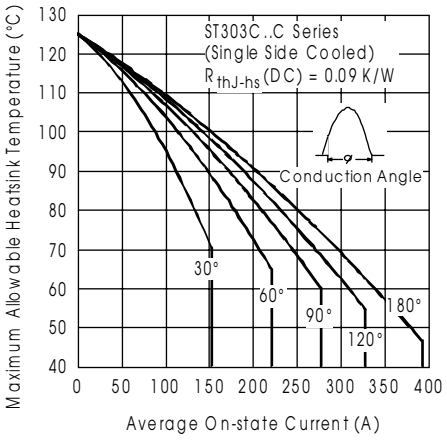


Fig. 1 - Current Ratings Characteristics

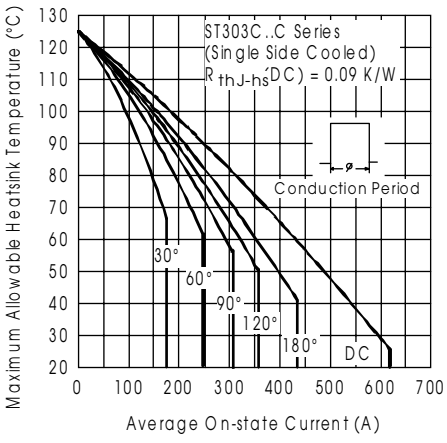


Fig. 2 - Current Ratings Characteristics

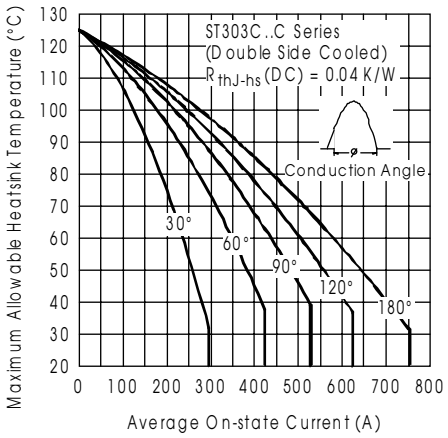


Fig. 3 - Current Ratings Characteristics

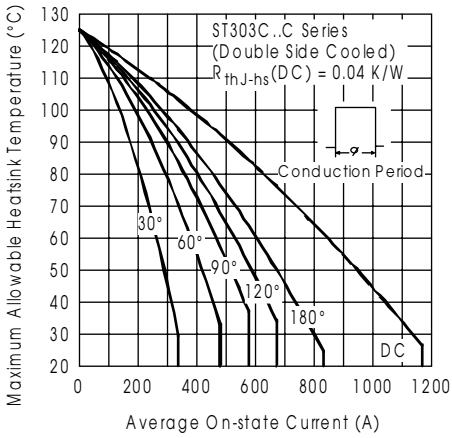


Fig. 4 - Current Ratings Characteristics

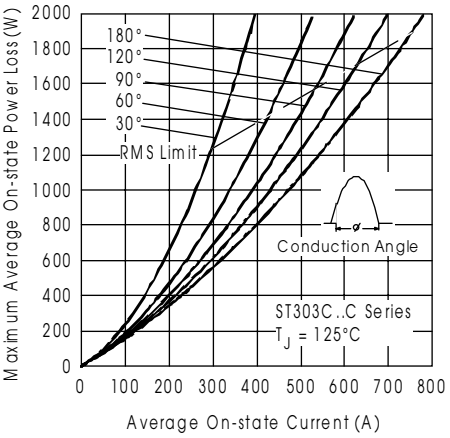


Fig. 5 - On-state Power Loss Characteristics

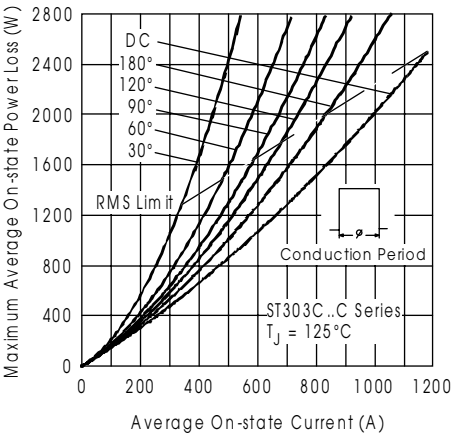


Fig. 6 - On-state Power Loss Characteristics

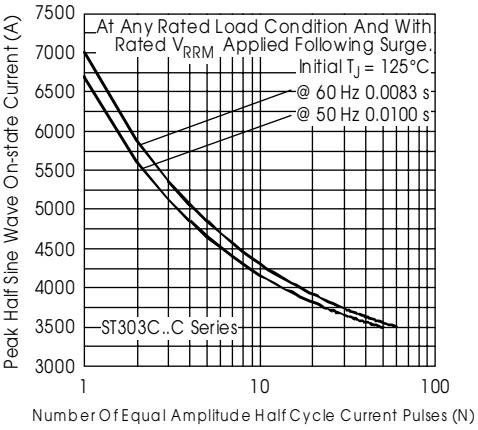


Fig. 7 - Maximum Non-repetitive Surge Current
Single and Double Side Cooled

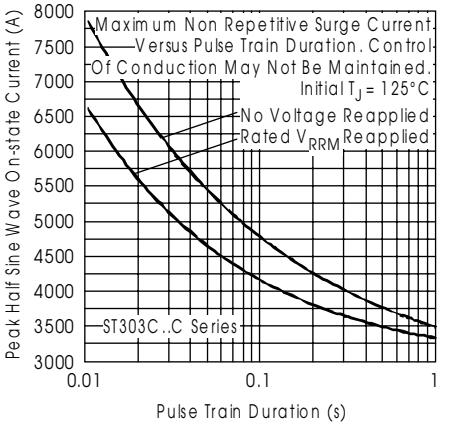


Fig. 8 - Maximum Non-repetitive Surge Current
Single and Double Side Cooled

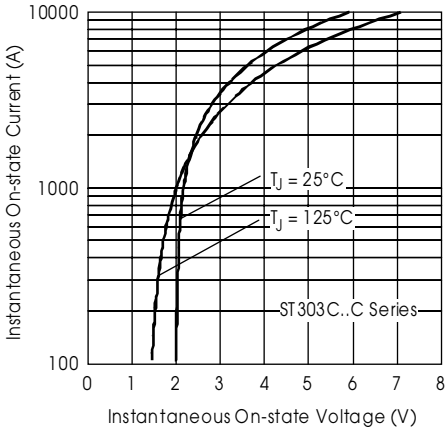


Fig. 9 - On-state Voltage Drop Characteristics

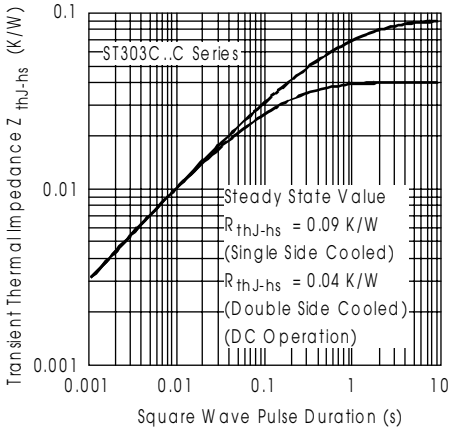


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

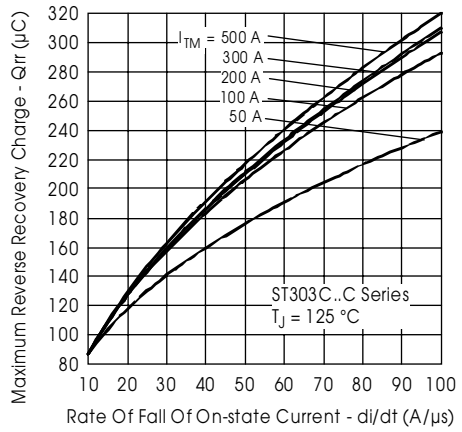


Fig. 11 - Reverse Recovered Charge Characteristics

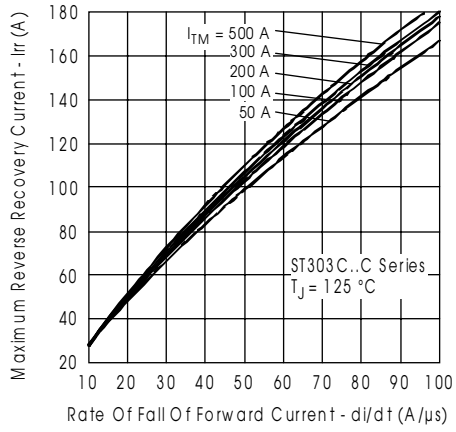


Fig. 12 - Reverse Recovery Current Characteristics

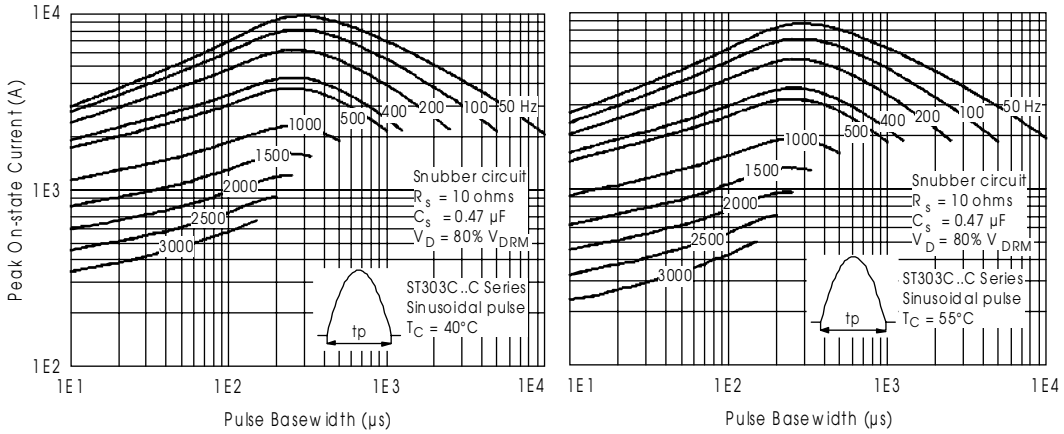


Fig. 13 - Frequency Characteristics

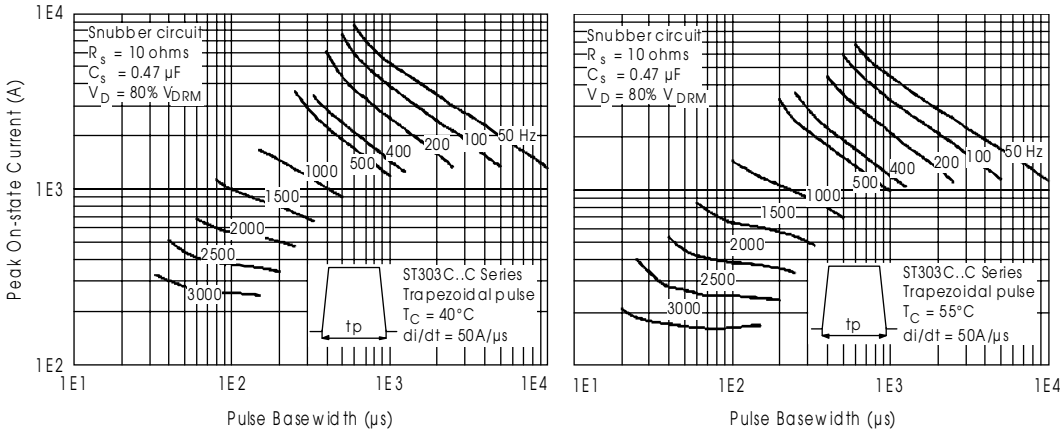


Fig. 14 - Frequency Characteristics

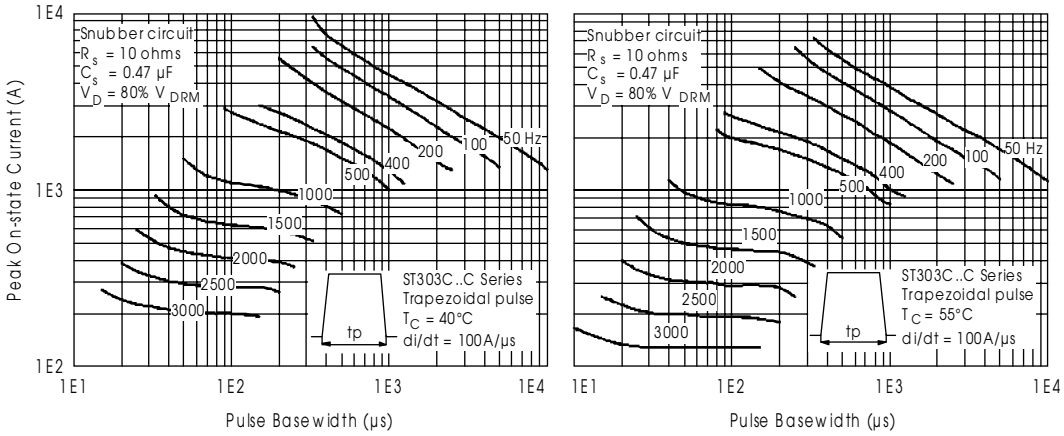


Fig. 15 - Frequency Characteristics

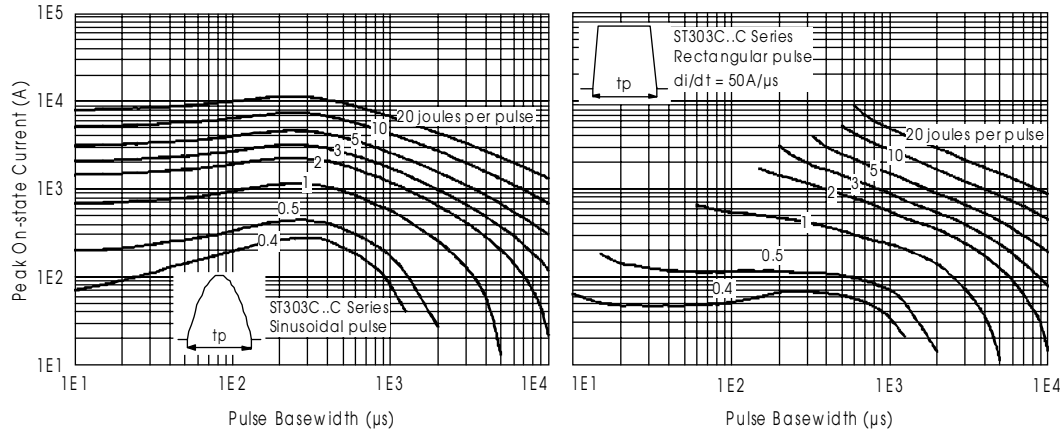


Fig. 16 - Maximum On-state Energy Power Loss Characteristics

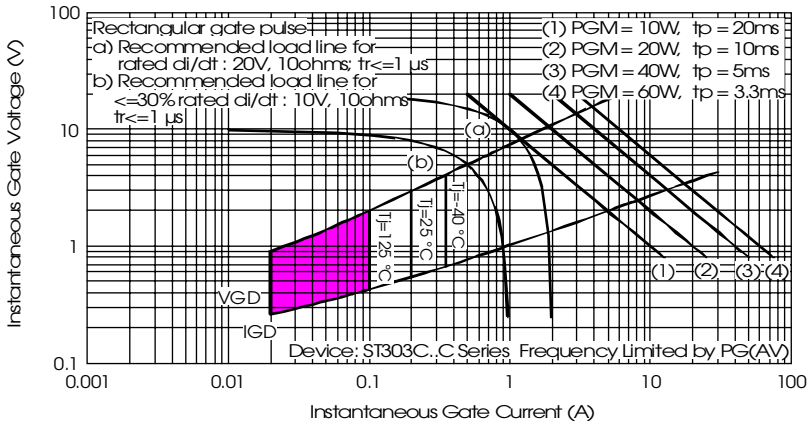


Fig. 17 - Gate Characteristics